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(54) **A radio receiving and gain control system**

(57) A radio receiver for a road vehicle detects at (6) the surrounding noise level and controls the output volume (3) in accordance with the surrounding noise level and also lowers the output volume in dependence upon the reduction in the received signal level. A microphone (6) located in the vehicle passenger compartment feeds a subtraction circuit (8) through a preamplifier (7). The negative input of subtraction circuit (8) is supplied with the audio signal from a power amplifier (4). A control circuit (12) controls a variable gain circuit (3) and receives inputs from a RF level detector (11) and an integration circuit (10) which is fed from the output of the subtraction circuit (8) through an envelope detector (9). As a result, even under the circumstances where the surrounding noise level is high and where the received signal level is low, the sound volume of the output sound which may contain many unwanted noises can be prevented from being raised.

FIG. 1

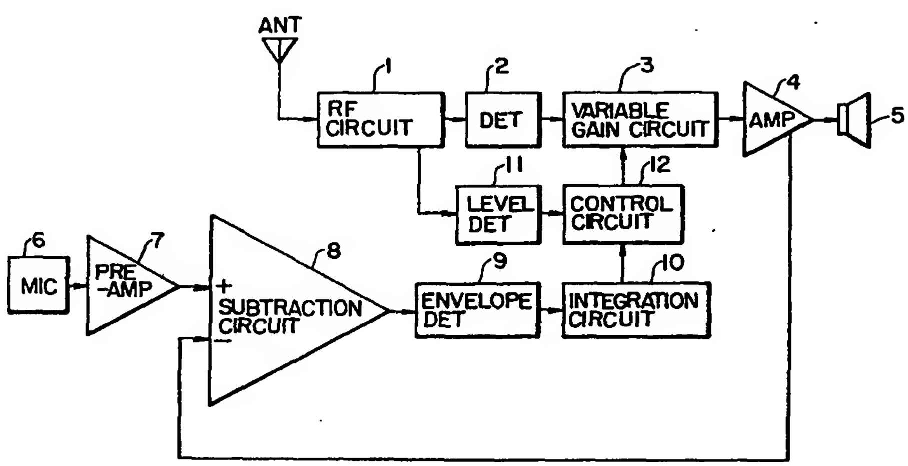

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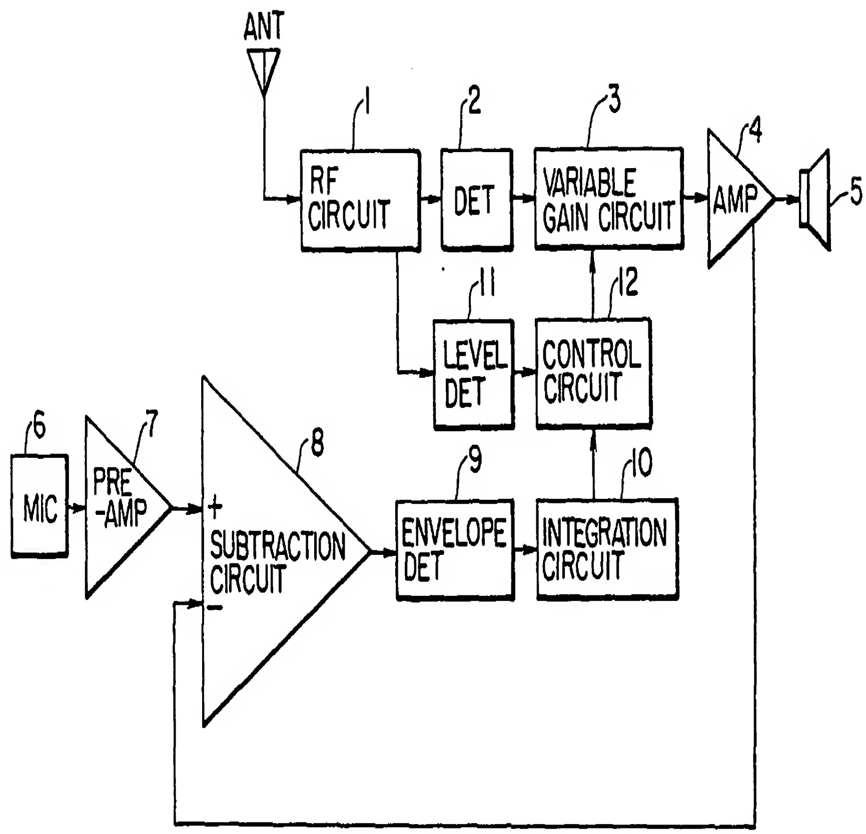
FIG. 1



1/6

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2/6

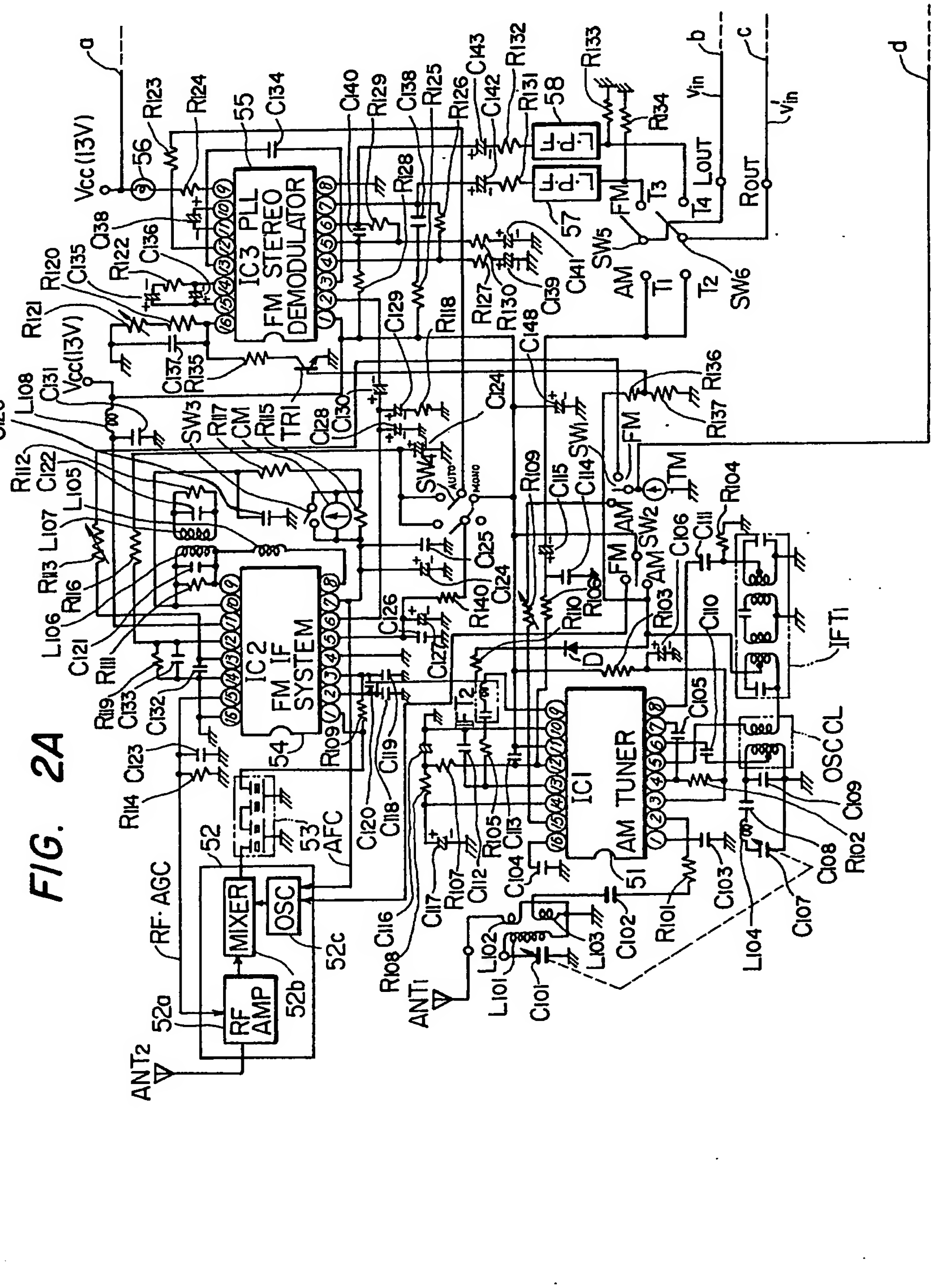
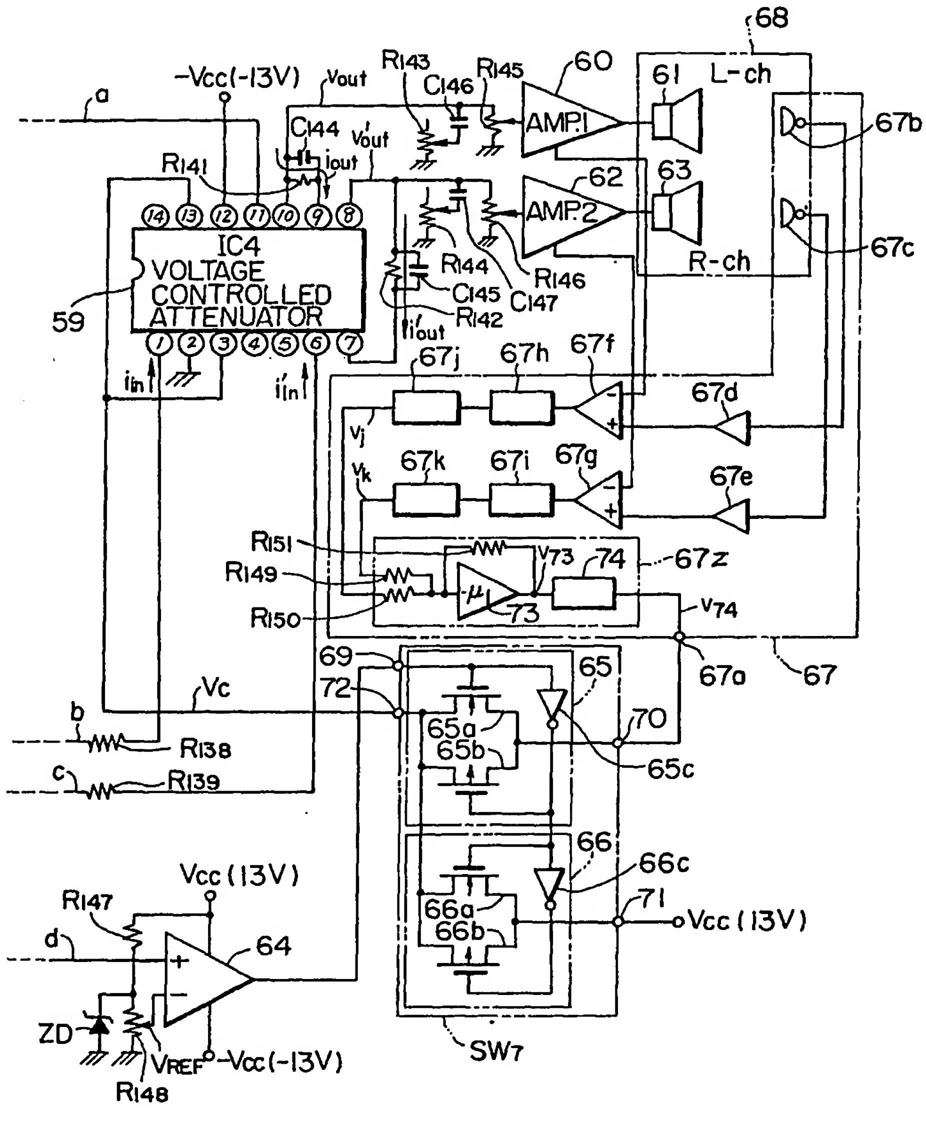


FIG. 2A

FIG. 2B


68
L-ch
R-ch
60
AMP.1
62
AMP.2
61
63
67b
67c
R143
C146
R145
-Vcc(-13V)
Vout
V'out
C144
iout
R141
a
IC4
VOLTAGE
CONTROLLED
ATTENUATOR
59
R144
C145
R142
R146
C147
i'out
iin
i'in
67j
67h
67f
67d
Vj
Vk
67k
67i
67g
67e
R151
R149
R150
V73
74
67z
73
V74
69
72
65
70
67a
67
Vc
b
R138
c
R139
65a
65b
65c
66
66c
66a
66b
71
Vcc (13V)
R147
d
64
ZD
VREF
-Vcc(-13V)
R148
SW7

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4/6

FIG. 3

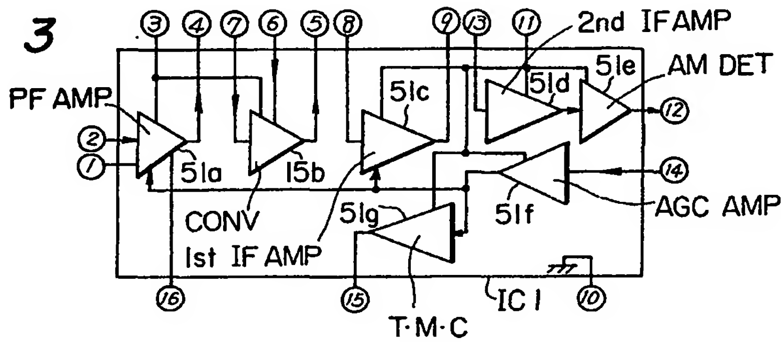


FIG. 6

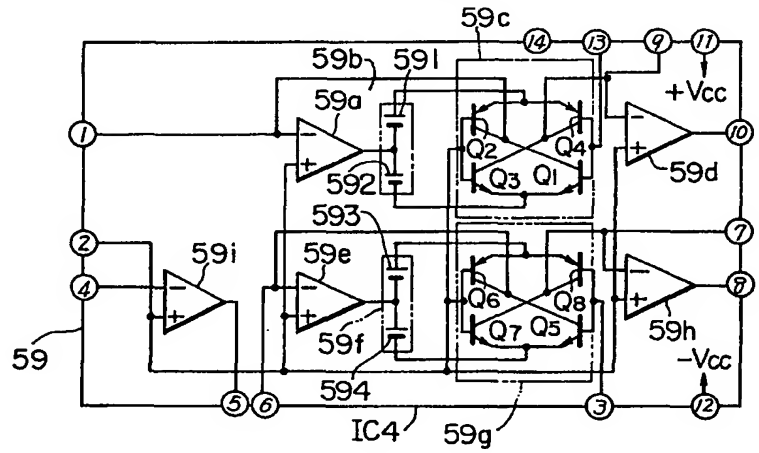


FIG. 7

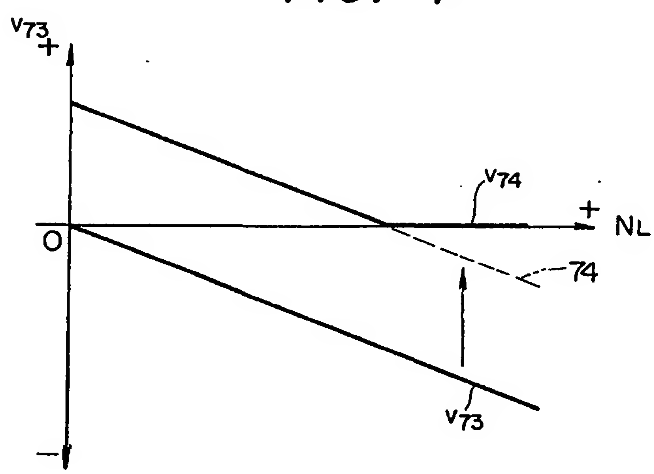
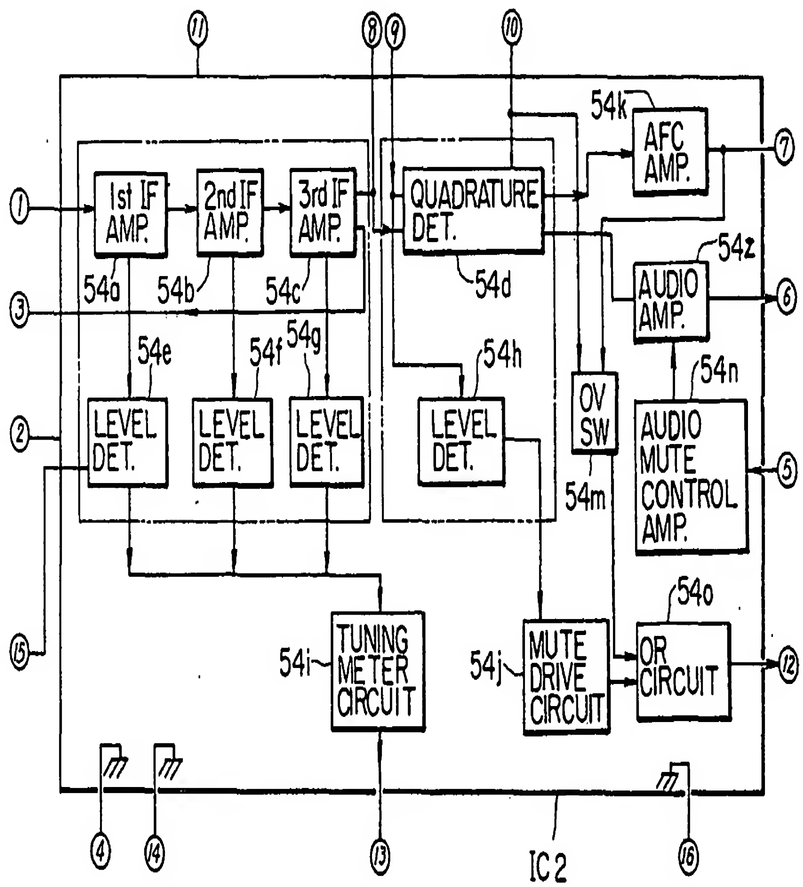


FIG. 4



5/6

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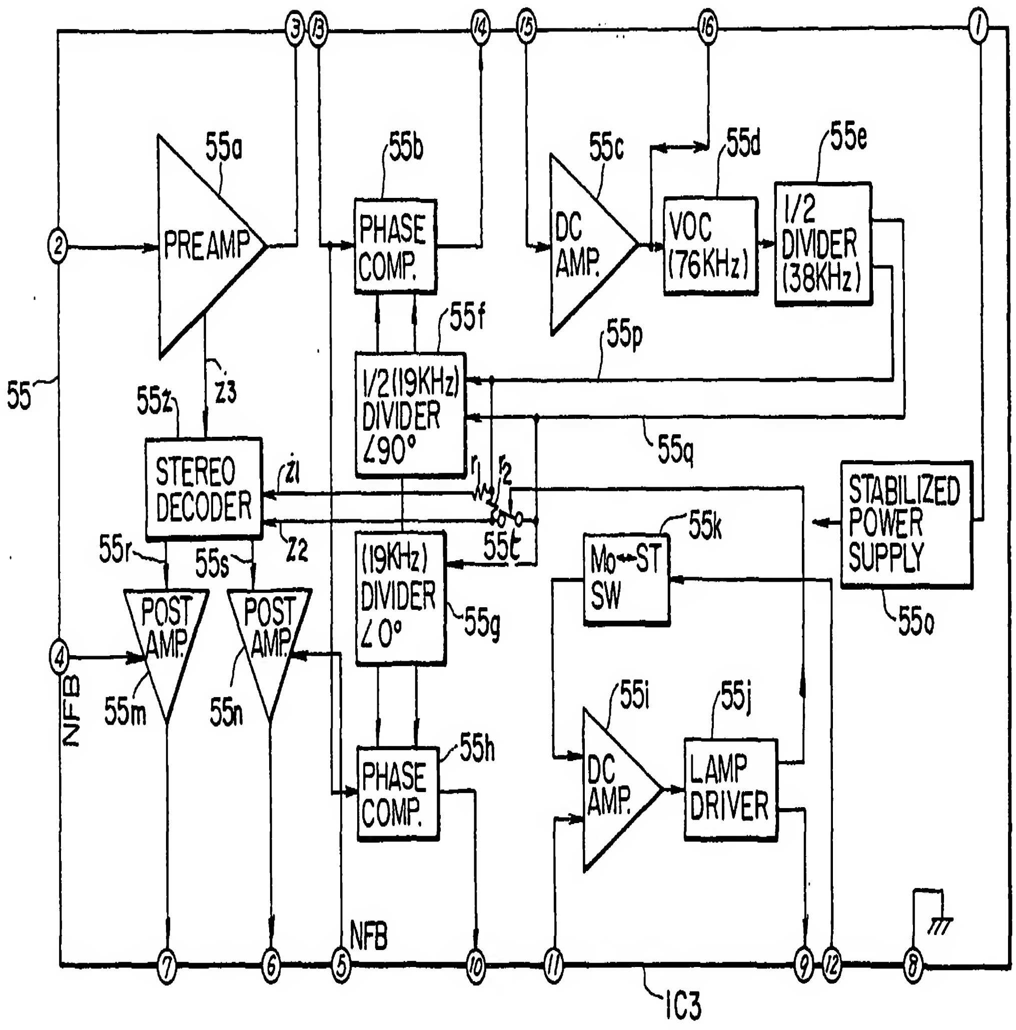
FIG. 5



6/6

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SPECIFICATION

A radio receiving reproducing system

The present invention relates to a radio receiving reproducing system which is suitable for installation in a vehicle such as a road vehicle.

In a sound field extending in the passenger compartment of a road vehicle, the surrounding noises other than the sounds generated by a radio receiver change greatly in volume.

In order to obviate this disadvantage, there has already been proposed an automatic sound volume control system for detecting those surrounding noises in order to control the output volume of the radio receiver proportionally in accordance with the noise level. Such a system has been disclosed in Japanese Laid-Open Patent Publication No. 82955/1979.

We have found that, if the control of the volume output is carried out in accordance with the automatic sound volume control system disclosed in the above referred to publication, then under the circumstances where the receiving condition is bad (e.g., in the case where the road vehicle is travelling in a tunnel), the output volume of the audio signals containing much unwanted interference and noise is augmented to provide a rather unpleasant effect for the listener, especially if he is listening to rather "delicate" music (e.g. a baroque concerto).

It is therefore an object of the present invention to provide a receiving reproducing system which can effect the automatic control of the sound volume without substantially affecting the quality of the reproduction.

According to the present invention there is provided a radio receiving reproducing system including: an antenna; a signal processing circuit adapted to obtain a detected output signal from a radio-frequency signal which is received by said antenna; a power amplifier for amplifying the detected output signal of said signal processing signal; a speaker adapted to be driven by the output signal of said power amplifier; a noise detector for detecting the surrounding noise level of a sound field; a variable gain circuit connected with said power amplifier in a manner to control the level of the output signal, which is to be supplied to said speaker, in proportion to the surrounding noise level of said sound field in response to the output signal of said noise detector; a received level detector for detecting the level which is dependent upon the received signal level of said antenna, the output of said received level detector lowering the level of the output signal of said power amplifier, in dependence upon the reduction in the received signal level.

The present invention will now be described in greater detail by way of examples, with reference to the accompanying drawings, wherein:—

Figure 1 is a block diagram showing a radio receiving reproducing system illustrating the basic principles of the present invention;

Figures 2A and 2B are block diagrams showing a preferred form of a radio receiving reproducing system;

Figure 3 is a block diagram showing the internal circuit of the first semiconductor integrated circuit used in the embodiment shown in Figs. 2A and 2B;

Figure 4 is a block diagram showing the internal circuit of the second semiconductor integrated circuit used in the embodiment shown in Figs. 2A and 2B;

Figure 5 is a block diagram showing the internal circuit of the third semiconductor integrated circuit used in the embodiment shown in Figs. 2A and 2B;

Figure 6 is a block diagram showing the internal circuit of the fourth semiconductor integrated circuit used in the embodiment shown in Figs. 2A and 2B; and

Figure 7 is a graph illustrating the relationship in the embodiment of Figs. 2A and 2B between the surrounding noise level in a sound field and the output voltage of a noise detector.

Referring to the block diagram of Fig. 1 which shows a radio receiving reproducing system for installation in a road vehicle, the radio frequency signal received by an antenna ANT is transmitted to the input of a radio-frequency circuit 1 which comprises a high-frequency tuning amplifier, a local oscillator, a mixer and an intermediate-frequency amplifier. A detector 2, for detecting the intermediate-frequency amplified output, has its output amplified by a low-frequency power amplifier 4 before being transmitted to a speaker 5. In order to control the output sound volume applied to the speaker 5 proportionally in accordance with the surrounding noise level of the sound field, the audio signal produced by the detector 2 is applied to the low-frequency power amplifier 4 through a variable gain circuit 3. The variable gain circuit 3 is controlled by the signal according to the surrounding noise level of the sound field.

The signal level which is dependent upon the noise level in the sound field, i.e., both the audio output generated by the speaker 5 and the surrounding noises are converted into electric signals by a microphone 6 before being amplified by a pre-amplifier 7. The output signal of the pre-amplifier 7 and the audio signal of the low-frequency power amplifier 4 are applied to a subtraction circuit 8, which comprises an operational amplifier, so that the audio signal is offset to generate only the surrounding noise component at the output of the subtraction circuit 8. The

output signal of this subtraction circuit 8 is converted into a D.C. signal by the action of an envelope detector 9 and an integrating circuit 10 so that the control signal of the variable gain circuit 3 is produced.

The noise detector, which comprises the microphone 6, the pre-amplifier 7, the subtraction circuit 8, the envelope detector 9 and the integration circuit 10, has its output signal transmitted under normal conditions to the variable gain circuit 3 through a control circuit 12. The gain of the variable gain circuit 3 is controlled in accordance with the level of the D.C. signal output from the integration circuit 10, so that the level of the audio signal which is applied to the speaker 5 is controlled in proportion to the surrounding noise level of the sound field.

Thus, in the case where the surrounding noise level of the sound field is high, the speaker 5 is fed with the audio output signal at a high level from the output terminal of the power amplifier 4. In the case where the surrounding noise level of the sound field is relatively low, the speaker 5 is fed with the audio output signal at a relatively low level.

In accordance with the inventive concept of the present invention, a received level detector 11 for detecting the level which is dependent upon the received signal level of the antenna ANT is especially connected with the high-frequency circuit 1. The output signal of the received level detector 11 is applied to the control circuit 12 whereby the output signal of the received level detector 11 controls the variable gain circuit 3 in dependence upon the reduction in the received signal level of the antenna ANT so that the level of the output signal of the power amplifier 4, which is applied to the speaker 5, is lowered.

It is preferable that the control circuit 12 lowers the level of the output signal of the power amplifier 4, which is impressed upon the speaker 5, only in the case where the output signal of the received level detector 11 falls below a given reference value. This reference value is so set that the control circuit 12 performs the operation to lower the level of the output signal which is applied to the speaker 5, in the case where the road vehicle is travelling in a tunnel in which case the received signal level of the antenna ANT is very weak so that the detected output of the detector 2 contains substantially only the noise component.

Thus, under the conditions of weak field strength signals but high surrounding noises, e.g., under the conditions one would expect in a tunnel, the sound volume output by the speaker can be muted without raising the output sound volume. As a result, the noise contained in the received signals can be prevented from being amplified at a high gain and transmitted to the speaker whereby an automatic sound volume control of high quality can be achieved.

It should be appreciated that the scope of the invention is not limited by the principle outlined above, so that it can cover the case where the gain of the variable gain circuit 3 is forcibly limited to a very low preset value by the output of the control circuit 12 or to the case where the transmission of the control signal is prevented from influencing the automatic sound volume control, so that the sound volume output by the speaker 5 is at a manually set low level.

The received level detector 11 can be used as a tuning meter driver if it is contained in the radio receiving reproducing system.

Referring now to the circuit diagrams shown in Figs. 2A and 2B, there is illustrated an FM/AM receiving reproducing system which is installed in a road vehicle.

The AM radio-frequency signal received by an AM antenna ANT_1 is applied to a second terminal of a first semiconductor integrated circuit IC1 through an AM antenna tuning circuit which comprises capacitors C_{101} and C_{102}, coils L_{101}, L_{102} and L_{103} and a resistor R_{101}. The first semiconductor integrated circuit IC1 is an integrated circuit for an AM tuner and can use the integrated circuit of type HA 1197 which is sold by us.

Fig. 3 shows the internal circuit block of a first preferred form of semiconductor integrated circuit IC1. This first semiconductor integrated circuit IC1 comprises an RF amplifier 51*a*, a frequency converter 51*b*, a first intermediate-frequency amplifier 51*c*, a second intermediate-frequency amplifier 51*d*, and AM detector 51*e*, and AGC (automatic gain control) amplifier 51*f*, a tuning meter circuit 51*g* and terminals 1 to 16 (hereinafter referred to as the first to sixteenth terminals of the integrated circuit). The RF amplifier 51*a* has its input terminal connected to a second terminal of the integrated circuit and its output terminal likewise connected to a fourth terminal of the integrated circuit. The RF amplifier 51*a* has its first and and sixteenth terminals earthed for A.C. signals. As shown in Fig. 2A, these first and and sixteenth terminals are connected to earth through capacitors C_{103} and C_{104}. The fourth terminal of the RF amplifier 51*a*, which acts as an output terminal, is connected through a capacitor C_{105} to a seventh terminal which acts as the input terminal of the frequency converter 51*b*. The fourth terminal is also connected with the third terminal through a resistor R_{102}.

The third terminal is supplied with a positive voltage from a voltage source V_{cc} through a filter which comprises a resistor R_{103} and a capacitor C_{106}. The RF amplifier 51a and the frequency converter 51*b* receive their power from the voltage source V_{cc}. Between the fifth and sixth terminals, there are connected an oscillation coil OSC CL, capacitors C_{107}, C_{108}, C_{109} and C_{110} and a coil L_{104}, which form part of the frequency converter 51*b* for determining the local oscillation

frequency of a local oscillator. The output terminal of the frequency converter 51*b* is connected to the fifth terminal of the integrated circuit.

The first intermediate-frequency amplifier 51*c* has its input and output terminals connected to the eighth and ninth terminals of the integrated circuit respectively. The eighth and fifth terminals are interconnected through the oscillation coil OSC CL, a first intermediate-frequency transformer IFT_1, a resistor R_{104} and a capacitor C_{111}.

The second intermediate-frequency amplifier 51*d* has its input terminal connected to the thirteenth terminal of the integrated circuit. The ninth and thirteenth terminals are interconnected through a second intermediate-frequency transformer IFT_2 and a resistor R_{105}. The thirteenth terminal is further connected to earth through a capacitor C_{112}. The output of the second intermediate-frequency amplifier 51*d* is applied to the input terminal of the AM detector 51*e* in the integrated circuit.

The twelfth terminal which acts as the output terminal of the AM detector 51*e* is connected to AM detection output terminals T_1 and T_2 through an output circuit which comprises a resistor R_{106} and capacitors C_{114} and C_{115}. The twelfth terminal is also connected to the voltage source V_{cc} through a capacitor C_{113}.

The AGC amplifier 51*f* which is constructed as a direct-current amplifier, has its input terminal connected to the fourteenth terminal of the integrated circuit. Between the twelfth and fourteenth terminals, there is connected a time constant circuit, which comprises resistors R_{107} and R_{108} and capacitors C_{116} and C_{117}, so that an AGC voltage is generated at the junction between the resistor R_{108} and the capacitor C_{117}. The AGC voltage thus generated is supplied to the fourteenth terminal (i.e., the input terminal of the AGC amplifier 51*f*) so that an AGC amplified voltage is generated at the output terminal of the AGC amplifier 51*f*. The AGC amplified voltage thus generated is applied to the RF amplifier 51*a* and the first intermediate-frequency amplifier 51*c* so that the automatic gain control operation is carried out while controlling the gains of the amplifiers 51*a* and 51*c*.

The tuning meter circuit 51*g* is an impedance converter of an emitter follower circuit type and has its input fed with the AGC amplified voltage so that a tuning meter drive voltage is generated at the fifteenth terminal. The tuning meter drive voltage thus generated is applied to a tuning meter TM through a variable resistor R_{109} and a first change-over switch SW_1.

The eleventh terminal is connected to the positive voltage source V_{cc}, to enable the first intermediate-frequency amplifier 51*c*, the second intermediate-frequency amplifier 51*d*, the AM detector 51*e*, the AGC amplifier 51*f* and the tuning meter circuit 51*g* to be supplied with power for their operation.

It should be noted that the AM tuner semiconductor integrated circuit of this kind is disclosed in detail in United States Patent Specification No. 4,030,035.

The FM radio-frequency signal received by an FM antenna ANT_2 is amplified by an RF amplifier 52*a* of an FM front end 52 and is applied to a mixer 52*b*. The mixer 52*b* is supplied with the local oscillation signal which is generated by a local oscillator 52*c*. Thus, the FM intermediate-frequency signal is obtained from the output terminal of the mixer 52*b* and is applied to a filter 53.

A second semiconductor integrated circuit IC2 is used for processing the FM intermediate-frequency signal and can make use of an integrated circuit of type HA1137W which is sold by us.

Fig. 4 shows the internal circuit block of the second semiconductor integrated circuit IC2. This second semiconductor integrated circuit IC2 comprises a first intermediate-frequency amplifier 54*a*, a second intermediate-frequency amplifier 54*b*, a third intermediate-frequency amplifier 54*c*, a quadrature detector 54*d*, a first level detector 54*e*, a second level detector 54*f*, a third level detector 54*g*, a fourth level detector 54*h*, a tuning meter circuit 54*i*, a mute drive circuit 54*j*, an AFC amplifier 54*k*, an audio amplifier 54*z*, a zero volt switch circuit 54*m*, an audio mute control amplifier 54*n*, an OR circuit 54*o*, and terminals 1 to 16 (hereinafter referred to as the first to sixteenth terminals of the second integrated circuit).

The second semiconductor integrated circuit IC2 has its first terminal, which acts as an input terminal, supplied with the FM intermediate-frequency signal through the filter 53. The FM intermediate-frequency signal is amplified by the first, second and third intermediate-frequency amplifiers 54*a*, 54*b* and 54*c* which are connected in cascade. These intermediate-frequency amplifiers operate as an FM limitter, by which the undesired AM signal component contained in the FM intermediate-frequency signal can be removed.

The second and third terminals are connected to earth through capacitors C_{118} and C_{119}, respectively, and a capacitor C_{120} is connected between the second and third terminals. A resistor R_{109} is connected between the first and third terminals so that negative feedback is obtained from the third intermediate-frequency amplifier 54*c* to the first intermediate-frequency amplifier 54*a*.

The second terminal is also connected to a second change-over switch SW_2 through a resistor R_{110} and a diode D.

The output signal of the third intermediate-frequency amplifier 54*c* is applied to the input of the quadrature detector 54*d*. A phase shift circuit is in the form of a network consisting of coils L_{105}, L_{106} and L_{107}, capacitors C_{121} and C_{122} and resistors R_{111} and R_{112} and which is connected to the eighth, ninth and tenth terminals of the second semiconductor integrated circuit IC2. The phase shift circuit constitutes the FM detector together with the quadrature detector 54*d*. The FM detector of this type is disclosed in IEEE TRANSACTIONS ON BROADCAST AND TELEVISION RECEIVERS, on pages 60 to 65, VOLUME BTR-13 NUMBER 3, which was published in November, 1967.

The first intermediate-frequency amplifier 54*a*, the second intermediate-frequency amplifier 54*b*, the third intermediate-frequency amplifier 54*c* and the ninth terminal are connected to the first level detector 54*e*, the second level detector 54*f*, the third level detector 54*g* and the fourth level detector 54*h*, respectively. These level detectors detect the peak value of the applied signals.

The outputs of the first, second and third level detectors 54*e*, 54*f* and 54*g* are applied to the tuning meter circuit 54*i*. The output of the tuning meter circuit 54*i* is applied to the thirteenth terminal of the integrated circuit. The tuning meter drive voltage from that thirteenth terminal is applied to the tuning meter TM through a variable resistor R_{113} and the first change-over switch SW_1. The intermediate-frequency amplifiers 54*a* to 54*c*, detector 54*d*, level detectors 54*e* to 54*h* and tuning meter circuit 54*i* are all disclosed in United States Patent Specification Nos. 3,673,499 and 3,701,022.

The other output of the first level detector 54*e* is applied as an automatic gain control voltage to the RF amplifier 52*a* of the FM front end 52 through the fifteenth terminal. Between the fifteenth terminal and earth, there is connected a parallel circuit comprising a resistor R_{114} and a capacitor C_{123}.

The quadrature detector 54*d* has its first output signal applied to the automatic frequency control amplifier 54*k* which in turn has its output signal applied to the local oscillator 52*c* of the FM front end 52 through the seventh terminal. Thus, since the frequency of the local oscillation signal obtained by the local oscillator 52*c* is controlled, the FM tuner can perform its stabilized tuning operation without being detuned from a preset radio-frequency signal.

The second output signal of the quadrature detector 54*d* is a stereo composite signal acting as the FM detection output signal and is transmitted to the sixth terminal through the audio amplifier 54*z*.

Both the voltage at the seventh terminal and the voltage at the tenth terminal are applied to the zero volt switch circuit 54*m*. The inter-terminal differential voltage V_7-V_{10} between the seventh and tenth terminals is reduced to zero volts at the S– characteristic centre frequency of the FM detector which comprises the phase shift circuit and the quadrature detector 54*d*. The absolute value of that inter-terminal differential voltage is proportional to the detuned frequency, and the positive and negative polarities of the differential voltage are determined in dependence upon whether the detuned frequency is higher or lower than the centre frequency. Thus, between the seventh and tenth terminals, there is arranged external to the integrated circuit, a network which comprises a centre meter CM, resistors R_{115} and R_{117}, capacitors C_{124}, C_{125} and C_{126}, and a third change-over switch SW_3.

In the case where the detuned frequency from the centre frequency is within a preset range, and in the case where the absolute value of the inter-terminal differential voltage between the seventh and tenth terminals is equal to or lower than a preset value, the zero volt switch circuit 54*m* feeds the OR circuit 54*o* with an output signal at a low level which is substantially equal to earth potential. When the frequency detuned from the centre frequency exceeds the range of the preset value, the zero volt switch circuit 54*m* feeds the OR switch 54*o* with an output signal at a high level.

The output of the fourth level detector 54*h* is applied to the mute drive circuit 54*j*. In the case where the level of the FM intermediate-frequency signal to be applied to the first terminal is equal to or higher than a preset value, the mute drive circuit 54*j* feeds the OR circuit 54*o* with the output signal at the low level. When the level of the FM intermediate-frequency signal to be applied to the first terminal becomes equal to or lower than the preset value so that the signal-to-noise ratio is substantially reduced, the mute drive circuit 54*j* feeds the OR circuit 54*o* with the output signal at the high level.

When at least one of the outputs of the zero volt switch circuit 54*m* and the mute drive circuit 54*j* generates the output voltage at the high level, the OR circuit 54*o* transmits the output voltage at the high level to the twelfth terminal. If both of the outputs of the zero volt switch circuit 54*m* and the mute drive circuit 54*j* are at the low level, the voltage at the twelfth terminal is at the low level.

The twelfth terminal is connected to the fifth terminal through a resistor R_{116}, a fourth change-over switch SW_4 and a resistor R_{140}. The junction between the resistor R_{116} and the fourth change-over switch SW_4 is connected to earth through a capacitor C_{124}, whereas the fifth terminal is connected to earth through parallel capacitors C_{126} and C_{127}.

The fifth terminal is connected to the control input terminal of the audio mute control amplifier 54*n*. When the fifth terminal is supplied with voltage at the high level, the output of the audio mute control amplifier 54*n* controls the gain of the audio amplifier 54*z* such that it is brought into a substantial zero condition. On the other hand, when the fifth terminal is supplied with voltage at the low level, the gain of the audio amplifier 54*z* is set to its maximum value.

The fourth change-over switch SW_4 is normally closed at the side marked AUTO. Under this condition, the voltage at the twelfth terminal is transmitted to the fifth terminal. As a result, either in the case where the frequency detuned from the centre frequency exceeds the preset range or in the case where the FM intermediate-frequency signal to be applied to the first terminal is equal to or lower than the preset value, the signal-to-noise ratio is set at a very low condition, the fifth terminal being supplied with voltage at the high level. Thus, in this case, the gain of the audio amplifier 54*z* is substantially reduced to zero. As a result, no sterio composite signal appears at the sixth terminal so that the audio mute operation is carried out. In the case where neither of the above referred to two conditions are satisfied, the voltage at the fifth terminal is at the low level so that the stereo composite output signal of the quadrature detector 54*d* is transmitted to the sixth terminal through the audio amplifier 54*z* which is set at its maximum value of gain.

The sixth terminal is connected to an output network which comprises capacitors C_{128}, C_{129} and C_{130}, and a resistor R_{118}. The fourth, fourteenth and sixteenth terminals are directly connected to earth.

The eleventh terminal is a voltage source supply terminal and is supplied with positive voltage from the voltage source V_{cc} through a filter which comprises a coil L_{108} and a capacitor C_{131}. The thirteenth terminal is connected to earth through a capacitor C_{132}, whereas the twelfth terminal is connected to earth through a parallel circuit comprising a capacitor C_{133} and a resistor R_{119}.

A third semiconductor integrated circuit IC3 is a semiconductor integrated circuit for PLL (phase-lock loop) FM stereo modulation and may consist of an integrated circuit of type HA1196 which is sold by us.

Fig. 5 shows the internal circuit block of the third semiconductor integrated circuit IC3. This third semiconductor integrated circuit IC3 comprises a pre-amplifier 55*a*, a first phase detector 55*b*, a first direct-current amplifier 55*c*, a voltage-controlled oscillator 55*d*, a first frequency divider 55*e*, a second frequency divider 55*f*, a third frequency divider 55*g*, a second phase detector 55*h*, a second direct-current amplifier 55*i*, a lamp driver 55*j*, a monaural-stereo switch circuit 55*k*, a stereo demodulator 55*z*, a first-post amplifier 55*m*, a second post-amplifier 55*n*, a stabilized power source supply circuit 55*o*, a switch 55*t*, and terminals 1 to 16 (hereinafter referred to as the first to sixteenth terminals of the third integrated circuit).

The second terminal which acts as the input terminal of the third semiconductor integrated circuit IC3 is fed with a stereo composite signal from the sixth terminal of the second semiconductor integrated circuit IC2. This stereo composite signal is amplified by the pre-amplifier 55*a* and is transmitted to the third terminal. A capacitor C_{134} is connected between the third terminal and the thirteenth terminal so that the stereo composite signal at the output terminal of the pre-amplifier 55*a* is transmitted to the inputs of the first and second phase detectors 55*b* and 55*h*.

Connected between fourteenth and fifteenth terminals is a low-pass filter which comprises a resistor R_{122} and capacitors C_{135} and C_{136}. The fifteenth terminal which acts as the input terminal to the first direct-current amplifier 55*c* is supplied with the low-frequency component of the output of the first phase detector 55*b* through the low-pass filter. The low-frequency component is amplified in a D.C. manner by the first D.C. amplifier 55*c* and is applied to the oscillation control terminal of the voltage-controlled oscillator 55*d*. The oscillation controlled terminal is connected to the sixteenth terminal of the third integrated circuit. The sixteenth terminal is connected to earth through a parallel network comprising a capacitor C_{137} and series connected resistors R_{120} and R_{121}. By adjusting the value of resistance of the resistor R_{121}, the free-running oscillation frequency of the voltage-controlled oscillator 55*d* is controlled. This free-running oscillation frequency should be set to such a frequency which is equal to a value several times as high as the frequency of a pilot signal contained in the stereo composite signal. The frequency of the pilot signal is 19 KHz, and by way of example the free-running oscillation frequency is preset at a frequency of 76 KHz which is equal to four times the frequency of the pilot signal.

Since the first frequency divider 55*e* generates an output signal having one half the frequency of the input signal, there are generated at two signal lines 55*p* and 55*q* two signals having a frequency of about 38 KHz, which are equal in amplitude but opposite in phase to each other.

The second frequency divider 55*f* feeds the first phase detector 55*b* with the output signal which has one half the frequency of the input signals on the signal lines 55*p* and 55*q*. The first phase detector 55*b* detects the difference between the phase of the pilot signal of 19 KHz, which is contained in the stereo composite signal obtained from the output terminal of the pre-amplifier 55*a*, and the phase of the output signal of about 19 KHz, which is obtained from the

output terminal of the second frequency divider 55*f*. Since the error output signal of the first phase detector 55*b* is transmitted to the voltage-controlled oscillator 55*d* through the low-pass filter and first direct-current amplifier 55*c*, the output signal of the first frequency divider at the two signal lines 55*p* and 55*q* has a substantially accurate frequency of 38 KHz and a phase which is synchronized with the phase of the pilot signal of 19 KHz. The closed loop, which consists of the first phase detector 55*b*, low-pass filter, first direct-current amplifier 55*c*, voltage-controlled oscillator 55*d*, first frequency divider 55*e* and second frequency divider 55*f*, constitutes the so-called "phase-lock loop (PLL)".

The output signal of 38 KHz, which is obtained from the first frequency divider 55*e* in the phase-lock loop, is fed in phase opposition to each through the two signal lines 55*p* and 55*q* to first and second input terminals z_1 and z_2 of the stereo demodulator 55*z*.

If the FM radio-frequency signal received by the FM antenna ANT_2 is an FM stereo broadcasting signal, there is fed out to the sixth terminal of the second semiconductor integrated circuit IC2 the stereo composite signal, in which there is contained a pilot signal having a frequency of 19 KHz having a preset amplitude.

On the other hand, in the case where the FM radio-frequency signal received by the FM antenna ANT_2 is an FM monaural broadcasting signal, not the stereo composite signal but the FM monaural detected output signal is supplied to the sixth terminal of the second semiconductor integrated circuit IC2. The latter FM monaural detected output signal no longer contains the pilot signal having a frequency of 19 KHz having a preset amplitude as described above.

In order to detect whether the FM radio-frequency signal received by the FM antenna ANT_2 is the FM stereo broadcasting signal or the FM monaural broadcasting signal, the existence of the pilot signal has to be detected. The third frequency divider 55*g* and the second phase detector 55*h*, which are arranged in the third semiconductor integrated circuit IC3, operate as the detector for detecting the existence of the pilot signal. It should be noted that the second phase detector 55*h* operates as a synchronous detector. During reception of the F M stereo broadcast signal, since the phase of the output signal of 38 KHz of the first frequency divider 55*e* in the phase-lock loop is in synchronism with that of the pilot signal of 19 KHz in the stereo composite signal, the phase of the output signal of 19 KHz of the third frequency divider 55*g* likewise synchronizes with that of the pilot signal of 19 KHz in the stereo composite signal under that condition. During reception of the FM stereo broadcast signal, consequently, the second phase detector 55*h* which acts as a synchronous detector detects the pilot signal of 19 KHz, which is contained in the stereo composite signal applied to the thirteenth terminal in synchronism with the frequency-divider output signal of 19 KHz, which is supplied from the third frequency divider 55*g* so that the tenth terminal is fed with the detected output signal which is proportional to the amplitude level of the pilot signal of 19 KHz.

During reception of the FM monaural broadcast signal, since the random noise component, which is contained in the FM monaural detected output signal applied to the thirteenth terminal, is applied to the second phase detector 55*h*, the average level of the output voltage of the second phase detector 55*h*, which is generated at a tenth terminal, is at earth potential.

A capacitor C_{138} is connected between the tenth terminal and the eleventh terminal, said capacitor C_{138} constituting a part of the low-pass filter. As a result, the low-frequency component of the output of the second phase detector 55*h* is transmitted to the eleventh terminal acting as the input terminal of the second direct-current amplifier 55*i*.

The stereo-monaural switch circuit 55*k* has its control input terminal connected to the twelfth terminal of the third intergrated circuit. In the case where the twelfth terminal is fed with the control voltage at a high level, the output signal of the stereo-monaural switch circuit 55*k* inhibits the amplification of the second direct-current amplifier 55*i*. On the contrary, in the case where the control voltage at the low level is applied to the twelfth terminal, the second direct-current amplifier 55*i* operates normally. The twelfth terminal is connected to the fourth change-over switch SW_4 through a resistor R_{123}.

The lamp driver 55*j* has an input threshold value which has to be exceeded by the output signal of the second direct-current amplifier 55*i* in order to energize a lamp 56. In the case where the output signal of the second direct-current amplifier 55*i* is at a level having a value which exceeds that threshold, the lamp driver 55*i* turns on the stereo indicator lamp 56 which is connected to the ninth terminal through a resistor R_{124}. The energization of the stereo indicator lamp 56 indicates that the FM tuner is receiving the FM stereo broadcast signal. On the contrary, the non-energization of the stereo indicator lamp 56 indicates not only that the FM tuner is receiving the FM monaural broadcast signal but also that it is operating under one of the two following conditions.

More specifically, in the case where the fourth change-over switch SW_4 is closed on the side marked MONO, the positive voltage of the voltage source V_{cc} is applied as the control signal at the high voltage level to the twelfth terminal through the switch SW_4 and the resistor R_{123}. Thus, since the output signal of the stereo-monaural switch circuit 55*k* inhibits the amplification of the second direct-current amplifier 55*i*, the lamp driver 55*j* partly turns off the stereo

indicator lamp 56, which is connected to the ninth terminal, and partly controls the switch 55*t*, which is connected between the second output signal line 55*q* of the first frequency divider 55*e* and the second input terminal z_2 of the stereo demodulator 55*z* into its open state. Since the output signal of 38 KHz appearing on the first output signal line 55*p* of the first frequency divider 55*e* drives the first and second input terminals z_1 and z_2 of the stereo demodulator 55*z* in in-phase mode through resistors r_1 and r_2, the stereo demodulation of the stereo demodulator 55*z* is not operational.

On the other hand, in the case where the fourth change-over switch SW_4 is closed on the side marked AUTO, the voltage at the twelfth terminal of the second semiconductor integrated circuit IC2 is applied to the twelfth terminal of the third semiconductor integrated circuit IC3 through the fourth change-over switch SW_4 and through the resistor R_{116}. Either in the case where the level of the FM intermediate-frequency signal applied to the first terminal of the second semiconductor integrated circuit IC2 becomes equal to or lower than a preset value so that the signal-to-noise ratio is substantially reduced or in the case where the detuned frequency from the S– characteristics centre frequency of the FM detector exceeds a preset value, there appears an output voltage of a high level at the twelfth terminal of the second semiconductor integrated circuit IC2. As a result, the gain of the audio amplifier 54*z* of the second semiconductor integrated circuit IC2 is reduced to substantially zero, and at the same time the lamp driver 55*j* of the third semiconductor integrated circuit IC3 partly turns out the stereo indicator lamp 56 and partly controls the switch 55*t*, which is connected between the second output signal line 55*q* of the first frequency divider 55*e* and the second input terminal z_2 of the stereo demodulator 55*z*, into its open condition.

On the other hand, in the case where the lamp driver 55*j* turns on the stereo indicator lamp 56, it moves the switch 55*t* to its closed state. The anti-phase output signal of 38 KHz at the first and second output signal lines 55*p* and 55*q* of the first frequency divider 55*e* drives the first and second input terminals z_1 and z_2 of the stereo demodulator 55*z* in phase opposition. The first and second input terminals z_1 and z_2 which are driven in phase opposition by the signal of 38 KHz so that the stereo demodulator 55*z* can achieve its stereo switching demodulation.

The other input terminal z_3 of the stereo demodulator 55*z* is fed with the stereo composite signal from the pre-amplifier 55*a*, and the first and second input terminals z_1 and z_2 are supplied with the switching signals of 38 KHz in phase opposition so that the stereo demodulator 55*z* outputs a left-channel demodulated output signal and a right-channel demodulated output signal to a first output terminal 55*r* and a second output terminal 55*s* respectively. A stereo demodulator of this switching type is disclosed in IEEE TRANSACTIONS ON BROADCAST AND TELEVISION RECEIVERS, on pages 58 to 73, VOLUME BTR–14 NUMBER 3.

Moreover, the semiconductor integrated circuit for FM stereo demodulation, which uses the phase-lock loop, is disclosed in the publication Electronics, (November 1971) on pages 62 to 66.

The left- and right-channel demodulated signals at the first and second output terminals 55*r* and 55*s* of the stereo demodulator 55*z* are amplified by the first and second post-amplifiers 55*m* and 55*n* respectively, and are transmitted to the seventh and sixth terminals respectively. The first and second post-amplifiers 55*m* and 55*n* are supplied with negative feedback signals on respective fourth and fifth terminals of the integrated circuit. The first, fourth and seventh terminals are connected with a network, which comprises resistors R_{125}, R_{126} and R_{127} and capacitors C_{138} and C_{139}, which enable the gain of the first post-amplifier 55*m* to be controlled. Likewise, the first, fifth and sixth terminals are connected with a network which comprises resistors R_{128}, R_{129} and R_{130} and capacitors C_{140} and C_{141}, which enable the gain of the second post-amplifier 55*n* to be controlled.

The left-channel demodulated output signal, which is obtained from the seventh terminal, is transmitted to a terminal T_3 through a capacitor C_{142}, a resistor R_{131} and a low-pass filter 57, whereas the right-channel demodulated output signal, which is obtained from the sixth terminal, is transmitted to a terminal T_4 through a capacitor C_{143}, a resistor R_{132} and a low-pass filter 58. The terminals T_3 and T_4 are connected to earth through resistors R_{133} and R_{134}, respectively. The first terminal of the third semiconductor integrated circuit IC3 is supplied with the positive voltage of the voltage source V_{cc} so that the stabilized power source supply circuit 55*o* feeds the stabilized operation voltage to the interior of the third semiconductor integrated circuit IC3.

The oscillation control terminal of the voltage-controlled oscillator 55*d* is connected to the sixteenth terminal of the integrated circuit and is connected to earth through a resistor R_{135} and the collector-emitter path of a transistor TR1. The AM side terminal of the second change-over switch SW_2 is connected to earth through resistors R_{136} and R_{137}. Moreover, the junction point of the resistors R_{136} and R_{137} is connected to the base electrode of the transistor TR1.

During an AM broadcast, since the second change-over switch SW_2 is closed on the AM side, there is generated at the junction point between the resistors R_{136} and R_{137} a divided voltage which is determined by dividing the positive voltage V_{cc} in the ratio of the resistances of the resistors R_{136} and R_{137}. The voltage thus divided renders the transistor TR1 conductive so that

the potential at the sixteenth terminal is at a relatively low level. Thus, the sixteenth terminal of the third semiconductor integrated circuit IC3 is preset at a relatively low potential so that the oscillating operation of the voltage-controlled oscillator 55*d* of the integrated circuit IC3 is inhibited. Thus, the circuit operation of the phase-lock loop in the third semiconductor integrated circuit IC3 is stopped during an AM broadcast.

During an FM broadcast, since the second change-over switch SW_2 is closed at the FM side, the positive voltage of the voltage source V_{cc} is fed to the local oscillator 52*c* in the FM front end 52 through the second change-over switch SW_2. Thus, the operation of the FM front end 52 is achieved.

During an AM broadcast, a fifth change-over switch SW_5 makes contact with the terminal T_1, and a sixth change-over switch SW_6 makes contact with the terminal T_2. The terminals T_1 and T_2 are fed with the AM detected output signal which is obtained from the twelfth terminal of the first semiconductor integrated circuit IC1.

During an FM broadcast, the fifth change-over switch SW_5 makes contact with the terminal T_3, and the sixth change-over switch SW_6 makes contact with the terminal T_4. The terminal T_3 is supplied with the left-channel demodulated output signal from the seventh terminal of the third semiconductor integrated circuit IC3. On the other hand, the terminal T_4 is supplied with the right-channel demodulated output signal from the sixth terminal of the third semiconductor integrated circuit IC3.

A fourth semiconductor integrated circuit IC4 shown in Fig. 2B is a semiconductor integrated circuit for a voltage-controlled attenuator, which is used as a variable gain circuit. This integrated circuit is disclosed in detail in British Patent Application No. 80.17243 published under Serial No.

The fourth semiconductor integrated circuit IC4 has first, sixth, tenth, eighth, thirteenth and third terminals which respectively act as a first signal input terminal, a second signal input terminal, a first signal output terminal, a second signal output terminal, a first control input terminal and a second control input terminal. The signal transmission from the first signal input terminal to the first signal output terminal can be controlled by the control voltage which is applied to the first control input terminal. Likewise, the signal transmission from the second signal input terminal to the second signal output terminal can be controlled by the second control voltage.

Referring now to Fig. 6, the fourth semiconductor integrated circuit IC4 includes a first operational amplifier 59*a*, a first level shift circuit 59*b*, a first transistor network 59*c*, a second operational amplifier 59*d*, a third operational amplifier 59*e*, a second level shift circuit 59*f*, a second transistor network 59*g*, a fourth operational amplifier 59*h* and a fifth operational amplifier 59*i*.

The first operational amplifier 59*a* has its inverting input terminal (–) and non-inverting input terminal (+) connected to the first and second terminals, respectively. The second terminal is connected to earth externally of the integrated circuit.

The output signal of the first operational amplifier 59*a* is applied to the first transistor network 59*c* through level shift elements 591 and 592 of the first level shift circuit 59*b*.

The first transistor network 59*c* comprises NPN transistors Q_1 and Q_3 and PNP transistors Q_2 and Q_4. The transistors Q_1 and Q_2 have their collector electrodes connected in common with the inverting input terminal (–) of the first operational amplifier 59*a*. The transistors Q_3 and Q_4 have their collector electrodes connected in common with the inverting input terminal (–) of the second operational amplifier 59*d*. The base electrodes of the transistors Q_2 and Q_3 are connected to the second terminal, whilst the base electrodes of the transistors Q_1 and Q_4 are connected to the thirteenth terminal.

The second operational amplifier 59*d* has its inverting input terminal (–) connected to the commoned collector electrodes of the transistors Q_3 and Q_4 and to the ninth terminal of the integrated circuit. The non-inverting input terminal (+) and the output terminal of the second operational amplifier 59*d* are connected with a second terminal and the tenth terminal, respectively.

The third operational amplifier 59*e* has its inverting input terminal (–) and non-inverting input terminal (+) connected with the sixth and second terminals, respectively. The output of the third operational amplifier 59*e* is connected to the second transistor network 59*g* through level shift elements 593 and 594 of the second level shift circuit 59*f*.

The second transistor network 59*g* comprises NPN transistors Q_5 and Q_7 and PNP transistors Q_6 and Q_8. The transistors Q_5 and Q_6 have their collector electrodes connected in common with the inverting input terminal (–) of the third operational amplifier 59*e*. The transistors Q_7 and Q_8 have their collector electrodes connected in common to the inverting input terminal (–) of the fourth operational amplifier 59*h*. The base electrodes of the transistors Q_6 and Q_7 are connected to the second terminal, whilst the base electrodes of the transistors Q_5 and Q_8 are connected to the third terminal.

The fifth operational amplifier 59*i*, which is not used in the present embodiment, is arranged

inside the integrated circuit and has its inverting input terminal (−), non-inverting input terminal (+) and output terminal connected with a fourth terminal, the second terminal and a fifth terminal, respectively.

Outside the integrated circuit, the first and sixth terminals are connected with the fifth change-over switch SW_5 and the sixth change-over switch SW_6, respectively, through resistors R_{138} and R_{139}. Also the thirteenth and third terminals are connected in common and supplied with a control voltage V_c.

A positive voltage $+V_{cc}$ and a negative voltage $-V_{cc}$ are supplied to the five operational amplifiers 59*a*, 59*d*, 59*e*, 59*h* and 59*i* through the eleventh and twelfth terminals, respectively.

A resistor R_{141} and a capacitor C_{144} are connected in parallel between the ninth and tenth terminals, whilst a resistor R_{142} and a capacitor C_{145} are connected in parallel between the seventh terminal and eighth terminals.

Such relationships as are expressed by the following equations hold for a first input signal current i_{in} which flows through the first terminal, a second input signal current i'_{in} which flows through the sixth terminal, a first output signal current i_{out} which flows through the ninth terminal, a second output signal current i'_{out} which flows through the seventh terminal, the absolute value $|V_c|$ of the control voltage V_c at the thirteenth and third terminals, a first input signal voltage v_{in} at one end of the resistor R_{138}, a second input signal voltage V'_{in} at one end of the resistors R_{139}, a first output signal voltage V_{out} at the tenth terminal, and a second output signal voltage v'_{out} at the eighth terminal:

$$i_{out} = i_{in}.\exp\frac{q(-|V_c|)}{kT} \quad \text{.........(1);}$$

$$i'_{out} = i_{in}.\exp\frac{q(-|V_c|)}{kT} \quad \text{.........(2);}$$

$$V_{in} = R_{138}.i_{in},\ V'_{in} = R_{139}.i'_{in} \quad \text{.........(3);}$$

and

$$v_{out} = R_{141}.i_{out},\ V'_{out} = R_{142}.i'_{out} \quad \text{......(4).}$$

As will be apparent from the above description, the first and second output signal voltages v_{out} and v'_{out} at the tenth and eighth terminals exponentially decrease with an increase in the absolute value $|V_c|$ of the control voltage V_c.

The first output signal voltage v_{out} is transmitted to the input terminal of a first power amplifier 60 through a tone control capacitor C_{146}, a variable resistor R_{143} and a sound volume adjusting variable resistor R_{145}. A first speaker 61 for the left hand channel of the stereo system is driven by the amplified output signal of the first power amplifier 60.

Likewise, the second output signal voltage v'_{out} is transmitted to the input terminal of a second power amplifier 62 through a tone control capacitor C_{147}, a variable resistor R_{144} and a sound volume adjusting variable resistor R_{146}. A second speaker 63 for the right hand channel of the stereo system is driven by the amplified output signal of the second power amplifier 62.

As shown in Figs. 2A and 2B, the tuning meter TM is connected to the non-inverting input terminal (+) of an operational amplifier 64 which acts as a voltage comparator. The inverting input terminal (−) of the operational amplifier 64 is supplied with a reference voltage V_{REF}. In order to generate this reference voltage V_{REF}, a resistor R_{147} and a zener diode ZD are connected in series between the positive voltage source $+V_{cc}$ and earth. A variable resistor R_{148} is connected in parallel with the both ends of the zener diode ZD so that the reference voltage V_{REF} can be obtained from the tap of the variable resistor R_{148}.

The output terminal of the operational amplifier 64 is connected to a control input terminal 69 of a seventh change-over switch SW_7. When the control input terminal 69 is supplied with a voltage at the high level, the seventh change-over switch SW_7 transmits only a voltage, which is applied to a first input terminal 70, to an output terminal 72. On the other hand, when the control input terminal 69 is supplied with a voltage at the low level, the seventh change-over switch SW_7 transmits only the voltage, which is applied to a second input terminal 71, to the output terminal 72. The seventh change-over switch SW_7 comprises a first switch unit 65 and a second switch unit 66.

These first and second switch units 65 and 66 are constituted by a CMOS analog switch. The first switch unit 65 comprises an N channel MOSFET 65*a* and a P channel MOSFET 65*b*, the source-drain paths of which are connected in parallel, and a first inverter 65*c* which is connected between the gate electrodes of the two MOSFETs 65*a* and 65*b*. Likewise, the second switch unit 66 comprises an N-channel MOSFET 66*a* and a P channel MOSFET 66*b*, the source-drain paths of which are connected in parallel and a second inverter 66*c* which is

connected between the gate electrodes of the two MOSFETs 66*a* and 66*b*.

The first input terminal 70 of the seventh change-over switch SW_7 is connected to an output terminal 67*a* of a noise detector 67 for detecting the noise in a sound field 68. The second input terminal 71 of the seventh change-over switch SW_7 is supplied with the positive voltage V_{cc} so as to carry out a forced attenuation.

A first microphone 67*b* and a second microphone 67*c* of the noise detector 67 are arranged in the sound field 68 extending in the passenger compartment of the road vehicle. The surrounding noises such as the engine noise from the engine compartment of the road vehicle or the road noises outside of the vehicle are transmitted to the sound field 68 or the passenger compartment of the vehicle. These surrounding noises exhibit relatively large changes.

The noise detector 67 further comprises a first pre-amplifier 67*d*, a second pre-amplifier 67*e*, a first operational amplifier 67*f*, a second operational amplifier 67*g*, a first envelope detector 67*h*, a second envelope detector 67*i*, a first integration circuit 67*j*, a second integration circuit 67*k* and an adder 67*z*. The adder 67*z* comprises resistors R_{149}, R_{150} and R_{151}, an inverting amplifier 73 and a level shift circuit 74.

The output signal of the first microphone 67*b* and the output signal of the second microphone 67*c* are transmitted through the first and second pre-amplifiers 67*d* and 67*e*, respectively, to the non-inverting input terminal (+) of the first operational amplifier 67*f* and the non-inverting input terminal (+) of the second operational amplifier 67*g*.

The output signal of the first operational amplifier 67*f* and the output signal of the second operational amplifier 67*g* are transmitted to the adder 67*z* through the first envelope detector 67*h* and the first integration circuit 67*j* and through the second envelope detector 67*i* and the second integration circuit 67*k*, respectively.

The adder 67*z* is in the form of an analog adder comprising resistors R_{149}, R_{150} and R_{151}, an inverting amplifier 73 and a level shift circuit 74. The adder 67*z* supplies the output terminal 67*a* with the output component which is the summation of the output of the first microphone 67*b* and the output of the second microphone 67*c*.

According to the preferred embodiment, the audio amplified signal of the first power amplifier 60 is applied to the inverting input terminal (−) of the first operational amplifier 67*f*, whereas the audio amplified signal of the second power amplifier 62 is applied to the inverting input terminal (−) of the second operational amplifier 67*g*. As a result, the first and second operational amplifiers 67*f* and 67*g* offset the audio amplified signal, which is contained in the output signal of the first pre-amplifier 67*d*, and the audio amplified signal, which is contained in the output signal of the second pre-amplifier 67*e*, in response to the audio amplified signals which are applied to their respective inverting input terminals (−). Thus, neither the audio signal of the first speaker 61 nor the audio signal of the second speaker 63 are substantially transmitted to the output terminal 67*a* of the noise detector 67, but the surrounding noise component in the sound field 68 or the passenger compartment are transmitted to the output terminal 67*a*.

Such relationships as are expressed by the following equation hold for a noise detection signal voltage v_j at the output terminal of the first integration circuit 67*j*, a noise detection signal voltage v_k at the output terminal of the second integration circuit 67*k*, and a voltage v_{73} at the output terminal of the inverting amplifier 73:

$$v_{73} = -\left[\frac{R_{151}}{R_{149}}v_k + \frac{R_{151}}{R_{150}}v_j\right] \ldots\ldots\ldots (5).$$

If the values of resistance of the resistors R_{149}, R_{150} and R_{151} are preset equal to one another, the voltage v_{73} is given by the following equation:

$$v_{73} = -(v_k + v_j) \ldots\ldots\ldots\ldots\ldots\ldots\ldots (6).$$

As a result, the relationship between the output voltage v_{73} of the inverting amplifier 73 and the surrounding noise level N_L of the sound field 68 or the passenger compartment is as illustrated in Fig. 7. The output voltage v_{73} in the case where the surrounding noise level N_L of the sound field 68 is low is substantially at zero, whereas the output voltage v_{73} in the case where the surrounding noise level N_L is high is at a negative potential level. The level shift circuit 74 feeds the output terminal 67*a* with an output voltage v_{74} which has its level shifted by a preset potential from the output voltage v_{73}, but the minimum potential of the output voltage v_{74} is limited to zero. The relationship between the output voltage v_{74} of the level shift circuit 74 and the surrounding noise level N_L of the sound field 68 is likewise illustrated in Fig. 7.

The first change-over switch SW_1 connected to the tuning meter TM is closed at the AM side during the AM broadcast reproduction and is closed at the FM side during the FM broadcast reproduction. As a result, the tuning meter TM is fed with either that component of the AM broadcast received signal, which is dependent upon the level of the AM detected output signal,

or that component of the FM broadcast received signal, which is dependent upon the level of the FM intermediate-frequency signal. In the case where the AM or FM broadcast signal under the preferred condition is being received, the tuning meter TM is supplied with the tuning meter drive voltage which is proportional to the level of the received signal.

Under this preferred condition, the tuning meter drive voltage is at a higher level than the reference voltage V_{REF} which is applied in advance to the inverting input terminal (–) of the operational amplifier 64 which acts as a voltage comparator. Under this condition, the output voltage at the output terminal of the operational amplifier 64, which is connected with the control input terminal 69 of the seventh change-over switch SW_7, is at the high level so that the seventh change-over switch SW_7 has its first switch unit 65 turned on and its second switch unit 66 turned off. As a result, the output voltage V_{74} at the output terminal 67*a* of the noise detector 67 is fed through the output terminal 72 of the seventh change-over switch SW_7 to the third and thirteenth terminals of the fourth semiconductor integrated circuit IC4.

Under this preferred condition, in the case where the surrounding noise level N_L of the sound field or the passenger room is high, the output voltage V_{74} of the noise detector 67, which is fed to the third and thirteenth terminals of the fourth semiconductor integrated circuit IC4, is substantially at zero so that the signal attenuation during the signal transmission from the first terminal to the tenth terminal and during the signal transmission from the sixth terminal to the eighth terminal is very low. As a result, in the case where the surrounding noise level N_L of the sound field 68 is high, the first and second speakers 61 and 63 are driven by the audio amplified output signal at the high level.

Under these conditions, when the surrounding noise level N_L of the sound field 68 or the passenger compartment is lowered, the output voltage v_{74} is raised to the high level so that the signal attenuation during the signal transmission from the first terminal to the tenth terminal and during the signal transmission from the sixth terminal to the eighth terminal is increased. As a result, when the surrounding noise level N_L of the sound field 68 is lowered, the first and second speakers 61 and 63 are driven by the audio amplified output signal at the low level.

On the contrary, in the case where the road vehicle is travelling in a tunnel, neither the AM radio-frequency signal nor the FM radio-frequency signal are received by the AM and FM antennae ANT_1 and ANT_2. As a result, the tuning meter TM is fed with a low voltage which is the noise component.

During the period when the road vehicle is within the tunnel, the only signal which appears in the AM detected output signal, which is obtained from the twelfth terminal of the first semiconductor integrated circuit and which is fed to the terminal T_1 of the fifth change-over switch SW_5 and to the terminal T_2 of the sixth change-over switch SW_6, is the noise component. Moreover, the audio muting operation is carried out at the second semiconductor integrated circuit IC2 by the control of the audio mute control amplifier 54*n* so that only the noise component appears at the sixth terminal. The noise component at the sixth terminal of the second semiconductor integrated circuit IC2 is transmitted to the second terminal of the third semiconductor integrated circuit IC3. This noise component transmitted to the second terminal does not contain any substantial pilot signal component at 19 KHz.

The stereo demodulator 55*z* of the third semiconductor integrated circuit IC3 does not carry out the stereo switching demodulation but transmits that noise component of the second terminal, which is amplified by the pre-amplifier 55*a*, to the first and second post-amplifiers 55*m* and 55*n*. As a result, the noise component, which is further amplified by the post-amplifiers, appears at the seventh and sixth terminals of the integrated circuit IC3 so that it appears at the terminal T_3 of the fifth change-over switch SW_5 and at the terminal T_4 of the sixth change-over switch SW_6.

The fifth and sixth change-over switches SW_5 and SW_6 are selectively closed on either the AM or FM side. In either selection, the noise component is transmitted to the first and sixth terminals of the fourth semiconductor integrated circuit IC4. If, under this condition, the seventh change-over switch SW_7 has its first switch unit 65 maintained in the conductive state and its second switch unit 66 maintained in the non-conductive state, an undesirable audible feeling results, as follows.

Specifically, the noise component, which is transmitted from the first terminal to the tenth terminal of the fourth semiconductor integrated circuit IC4, and the noise component, which is transmitted from the sixth terminal to the eighth terminal, are amplified by the first and second power amplifiers 60 and 62, respectively, and are then transmitted to the first and second speakers 61 and 63, respectively. When the surrounding noise level N_L of the sound field 68, which is dependent upon the engine noise or the road noise, is raised, the output voltage v_{74} at the output terminal 67*a* of the noise detector 67 is lowered to earth or zero potential so that the attenuation during the signal transmission from the first terminal to the tenth terminal and during the signal transmission from the sixth terminal to the eigth terminal is lowered. In this case, an undesired phenomena results in that the noise voltages dependent upon the noise components supplied to the first and sixth terminals are generated at high levels from the first

and second speakers 61 and 63, respectively.

In order to prevent these undesirable effects, the tuning meter drive voltage of the tuning meter TM is applied to the non-inverting input terminal (+) of the operational amplifier 64. During the period whilst the road vehicle is within the tunnel, the tuning meter drive voltage falls to such a low value that its level becomes equal to or lower than the reference voltage V_{REF}.

As a result, the output voltage of the operational amplifier 64, which is connected with the control input terminal 69 of the seventh change-over switch SW_7, takes a low level so that the seventh change-over switch SW_7 has its first switch unit 65 rendered non-conductive and its second switch unit 66 rendered conductive. Thus, the positive power source voltage $+V_{co}$, which is fed to the second input terminal 71 of the seventh change-over switch SW_7, is fed through the output terminal 72 of that switch SW_7 to the third and thirteenth terminals of the fourth integrated circuit IC4, so that the signal attenuation during the signal transmission from the first terminal to the tenth terminal of the integrated circuit IC4 and during the signal transmission from the sixth terminal to the eighth terminal becomes substantially high.

Thus during the period whilst the vehicle is travelling in the tunnel, little noise voltage is generated from the first and second speakers 61 and 63 so that the undesired effects described above can be prevented.

CLAIMS

1. A radio receiving reproducing system including: an antenna; a signal processing circuit adapted to obtain a detected output signal from a radio-frequency signal which is received by said antenna; a power amplifier for amplifying the detected output signal of said signal processing signal; a speaker adapted to be driven by the output signal of said power amplifier; a noise detector for detecting the surrounding noise level of a sound field; a variable gain circuit connected with said power amplifier in a manner to control the level of the output signal, which is to be supplied to said speaker, in proportion to the surrounding noise level of said sound field in response to the output signal of said noise detector; a received level detector for detecting the level which is dependent upon the received signal level of said antenna, the output of said received level detector lowering the level of the output signal of said power amplifier, in dependence upon the reduction in the received signal level.

2. A radio receiving reproducing system according to Claim 1, further including a control circuit supplied with the output signal of said received level detector, wherein said control circuit lowers the level of the output signal of said power amplifier, only in the case where the output signal of said received level detector becomes equal to or lower than a given value.

3. A radio receiving reproducing system according to Claim 2, wherein said noise detector includes a microphone, a pre-amplifier for amplifying the output signal of said microphone, a subtraction circuit supplied with the output signal of said pre-amplifier and the audio signal of said power amplifier, a detector connected with the output of said subtraction circuit, and an integration circuit connected with the output of said detector, the output signal of said integration circuit being fed to said control circuit.

4. A radio receiving reproducing system according to Claim 2 or 3, wherein said received level detector is also utilized as a tuning meter driver.

5. A radio receiving reproducing system according to any one of the preceding claims, wherein at least said antenna, said speaker and said noise detector are carried on a road vehicle.

6. A radio receiving reproducing system according to Claim 1, wherein said antenna includes an AM antenna and an FM antenna; wherein said signal processing circuit includes and AM tuner for obtaining an AM detected output signal from the AM radio-frequency signal which is received by said AM antenna, an FM front end for obtaining an FM intermediate-frequency signal from the FM radio-frequency signal which is received by said FM antenna, an FM intermediate-frequency signal processing circuit for obtaining an FM detected output signal from said FM intermediate-frequency signal, and an FM stereo demodulator for obtaining a left hand channel demodulated output signal and a right hand channel demodulated output signal from said FM detected output signal.

7. A radio receiving reproducing system according to Claim 6, wherein said power amplifier includes a first power amplifier and a second power amplifier and wherein said speaker includes a first speaker and a second speaker which are driven by the output signal of said first power amplifier and the output signal of said second power amplifier, respectively.

8. A radio receiving reproducing system according to Claim 6 or 7, wherein said variable gain circuit includes a voltage-controlled attenuator having its signal transmission from a first input terminal to a first output terminal controllable by the control voltage, which is supplied to a first control input terminal, and its signal transmission from a second input terminal to a second output terminal controllable by the control voltate which is supplied to a second control input terminal, the first input terminal and the second input terminal of said voltage-controlled attenuator being selectively supplied with either the AM detected output signal, which is obtained from said AM tuner, or the left hand or right hand channel demodulated output signal

which is obtained from said FM stereo demodulator, the first output terminal and the second output terminal of said voltage-controlled attenuator being connected with the input terminal of said first power amplifier and the input terminal of said second power amplifier, respectively.

9. A radio receiving reproducing system according to any one of the preceding claims 6 to 8, wherein said received level detector includes a tuning meter circuit in said AM tuner and a tuning meter circuit in said FM intermediate-frequency signal processing circuit, and wherein said control circuit includes a voltage comparator to be fed with a drive voltage from the tuning meter and a reference voltage which corresponds to a given value.

10. A radio receiving reproducing system according to Claim 9, wherein said control circuit further includes a change-over switch having its first input terminal fed with the output voltage of said noise detector, its second input terminal fed with a control voltage for forced attenuation, and its output terminal connected with the first and second control input terminals of said voltage-controlled attenuator.

11. A radio receiving reproducing system according to Claim 10, wherein the output of said voltage comparator controls said change-over switch, in the case where said tuning meter drive voltage is higher than said reference voltage, to supply the output voltage of said noise detector to the first and second control input terminals of said voltage-controlled attenuator, and to supply said control voltage for forced attenuation to the first and second control input terminals of said voltage-controlled attenuator in the case where said tuning meter drive voltage is lower than said reference voltage.

12. A radio receiving reproducing system constructed and arranged to operate substantially as herein described with reference to and as illustrated in the accompanying drawings.

13. A road vehicle equipped with a radio receiving reproducing system according to any one of the preceding claims.

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